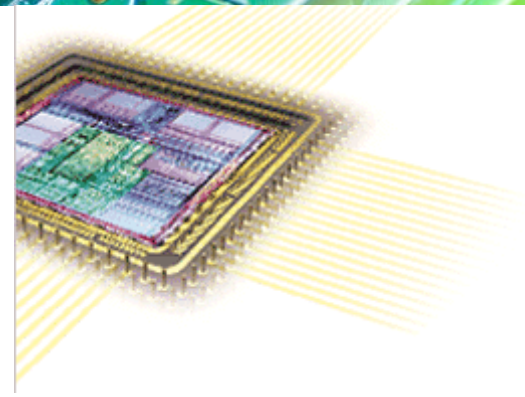


ntRSC_IESS

IESS Reed Solomon Codec



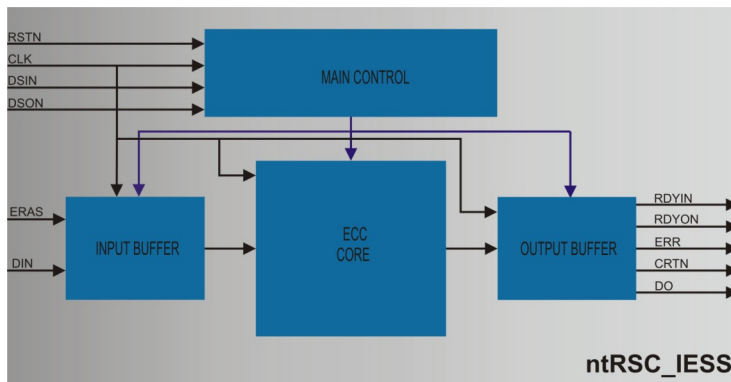
In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system strongly depends on the amount of redundancy as well as on the coding algorithm itself. ntRSC_IESS core is a highly integrated solution implementing a time-domain Reed-Solomon Forward Error Correction algorithm. The core supports several programming features including codeword size, error threshold, number of parity bytes, reverse or forward order of the output, mode of operation (encode, decode or pass-through), shortened code support, erasures or error only decoding. Very low latency, high speed, simple interfacing and programmability make this core ideal for many applications including Intelsat IESS-308, DTV, DBS, ADSL, Satellite Communications, High performance modems and networks.

Applications

The ntRSC_IESS core can be used in a variety of applications, including:

- Intelsat Earth Stations (IESS-308).
- Digital Television (DTV).
- Direct Broadcast Satellite (DBS).
- Asymmetric Digital Subscriber Lines (ADSL).
- Satellite Communications.
- High performance modems and networks.

Block Diagram



Features

HIGH PERFORMANCE

- Polynomial compliant to Intelsat IESS-308; RTCA DO-217 Appendix F, Revision D Standard.
- High throughput rate.

FLEXIBILITY

- Fully programmable to correct from 1 to 10 error bytes or 20 erasure bytes per block.
- Configurable odd or even number of check bytes.
- Codeword lengths can be programmed from 3 to 255 bytes.
- Can be configured in encode, decode or pass-through mode of operation.
- Outputs corrected bytes or correction vectors in forward or reverse order.
- Supports continuous or burst data transfer.
- Supports programmable error threshold to help in determining channel performance.

SYSTEM INTERFACE

- Byte wide synchronous I/O ports with internal buffering.
- Dedicated control pins enable non-continuous system data flow.

OTHERS

- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources	Fmax (MHz)
Xilinx	Virtex-5	2510 CLB Slices ¹ / 5 Block RAMs	134
Xilinx	Virtex-4	4800 CLB Slices ¹ / 5 Block RAMs	105
TSMC	0.18 um	40 K gates ² / 12 K RAM bits	180

1) Each Virtex-5 CLB Slice contains four LUTs and four flip-flops.

Each Virtex-4 CLB Slice contains two LUTs and two flip-flops.

2) Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntRSC_IESS core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- C++ model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntRSC_IESS core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.