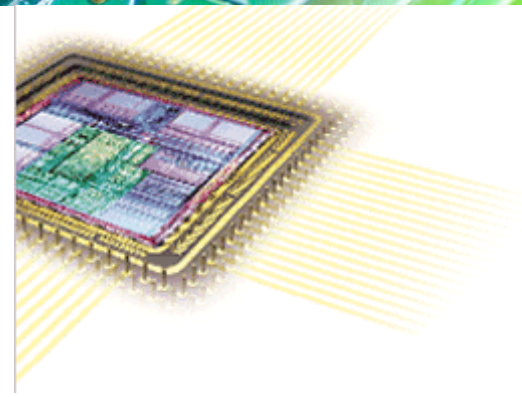


ntI2C_M I2C Master Controller



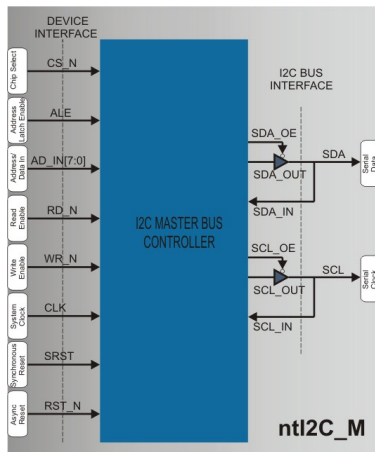
The ntI2C_M is an I2C-bus multi-master interface controller developed as a VHDL synthesizable block. The ntI2C_M provides a cost-effective solution for a wide range of applications that require a low-cost serial communication channel. It provides a serial interface between a device and an I2C-bus, where an external host processor is controlling the device via the I2C-bus and the I2C master interface unit. The I2C-bus communication protocol is ideal for applications where low power consumption and noise tolerance is of crucial importance as well as in cases where low device interconnection overhead is strongly required. These features render the I2C-bus an ideal solution for portable systems and battery-powered applications. The I2C standard is a multi-master bus that handles collision detection and arbitration thus preventing data corruption if two or more masters attempt to control the bus simultaneously. Practically the I2C-bus interface is a parallel to serial and serial to parallel converter. The serial data received from I2C-bus is converted to parallel for the CPU device. The parallel data received from the CPU or any other target device is converted to serial form for transmission on the I2C-bus. The ntI2C_M core is available in VHDL and is synthesizable to any FPGA or ASIC technology. The core can be easily customized for specific customer needs and is provided with test-benches and full documentation.

Applications

The ntI2C_M core can be used in a variety of applications, including:

- Wireless broadband – IEEE 802.16 Suitable for a wide range of applications in telecom systems, industrial and consumer electronics, which require a cost effective serial communication channel.
- Suitable for peripherals with embedded microprocessors or micro-controllers. GPON (G.984).
- Flexible parallel interface compatible with a wide variety of micro-controllers. DVB (ETS 300-429 – Cable).

Block Diagram



- Supports clock stretching and wait state generation.
- Start-bit, Stop-bit, Repeated start-bit and acknowledge-bit generation.
- Multi-master operation.
- 8051 microprocessor I/F supported.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntI2C_M core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntI2C_M core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

Features

- Supports 3 transmission speeds:
 - normal: 100 kbps
 - fast: 400 kbps
 - high speed: 3.5 Mbps
- Programmable clock frequency.
- Programmable acknowledge bit.
- RAM data packet buffer included with parameterized length.
- Interrupt driven data transfers.