ComLab ©

A new paradigm towards communication systems hardware emulation.

ComLab is a cost efficient highly integrated development environment (IDE) that enables a system designer to rapidly build, configure and evaluate in real-time the performance of complex telecommunication systems. It is comprised of a Xilinx FPGA based board for the real-time HW emulation, a sophisticated application SW with interactive GUI capabilities for configuration, control and monitoring purposes as well as a rich portfolio of highly optimized telecom subsystem silicon IPs. ComLab platform is ideal for proof-of-concept rapid prototyping as well as an intuitive educational tool for engineers.

Applications

► Fast and efficient modeling and development of complex telecom systems.

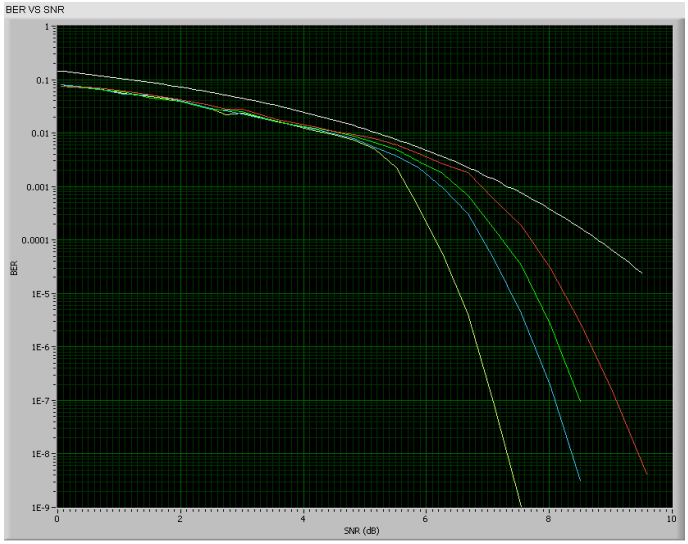
► Proof-of-concept rapid prototyping.

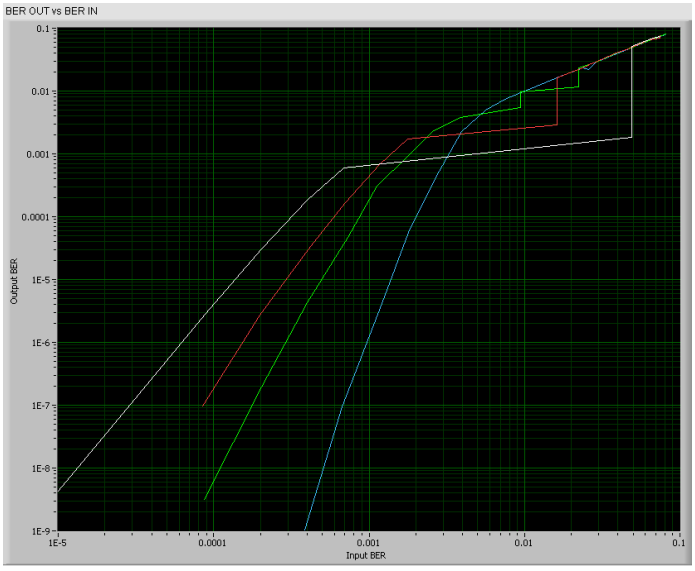
► In-circuit emulation.

► R&D telecom engineers training.

► Educational tool for universities.

► Low-volume production.





Features

► Rich portfolio of silicon optimized telecom subsystem libraries.

►Fully configurable system parameters.

►Sophisticated application SW for efficient real-time performance evaluation and configuration.

► Supports graphical display capabilities of key characteristics such as BER vs SNR graphs, BER In vs BER out graphs, Eye-Diagrams, Constellation Diagrams etc.

► Results are displayed in both graphical and tabular formats with print out, save and load capabilities.

► Can operate in a stand-alone mode or in an in-circuit emulation mode.

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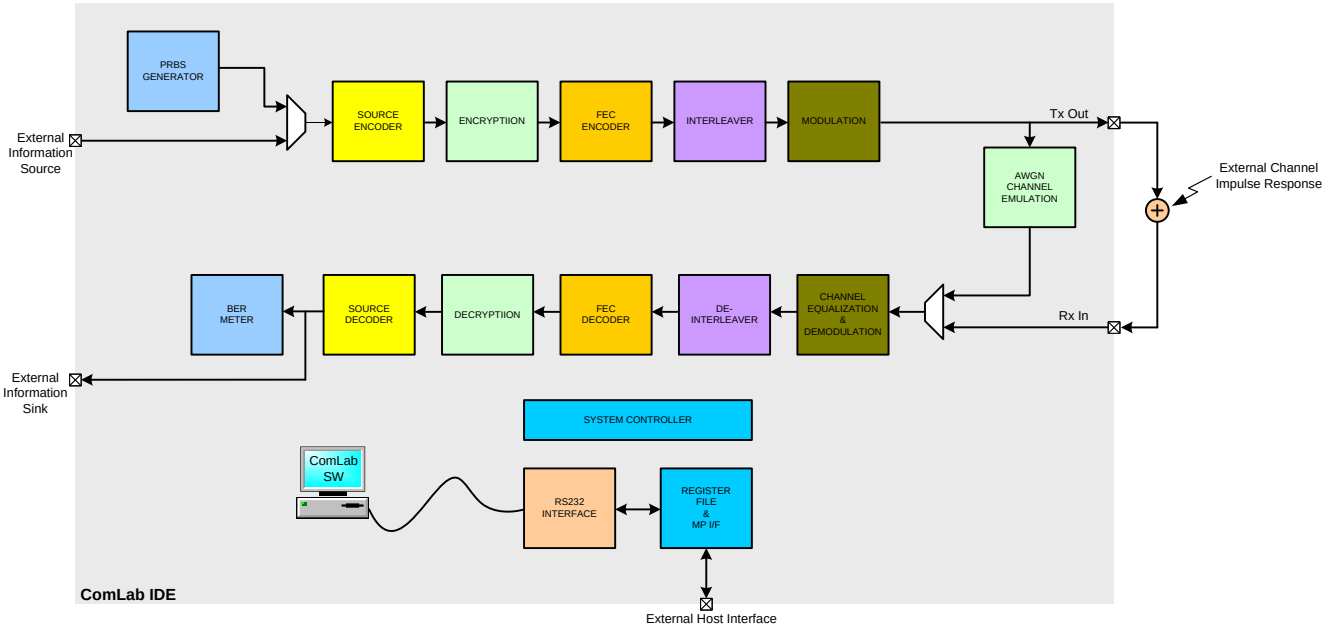

Technical Data

Telecom subsystem silicon IP libraries	■ Forward Error Correction (Reed Solomon, BCH, Viterbi, RS-Viterbi concatenated, Turbo product code) ■ Interleaving/Deinterleaving (Block, Convolutional) ■ Channel equalization (LMS based) ■ Modulation (PSK, QAM) ■ Soft output demodulation (LLR based) ■ Source coding (ITU-T G.726, G.711) ■ Encryption/Decryption (AES, RC4) ■ AWGN channel emulation
Graphical Display	■ BER vs SNR graphs ■ BER In vs BER Out graphs ■ Eye Diagrams ■ Constellation Diagrams
Configuration parameters	■ Codeword sizes ■ Error correction capability ■ Interleaving profile ■ Modulation level ■ SNR measurement range ■ SNR measurement step ■ BER threshold ■ Number of soft bits per symbol ■ PRBS generator length
Hardware emulator platform	Spartan3 Xilinx FPGA based
System requirements	Windows XP and higher, RS-232 interface.

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