

Noesis Technologies specializes in the design, development and marketing of VHDL and Verilog high quality, cost efficient, telecom IP cores that are key components to the most sophisticated System-On-Chips. With our leading edge expertise on DSP algorithm development and implementation we provide highly efficient solutions on complex signal processing telecom systems. Our IP cores are silicon proven and technology independent for easy porting to any target semiconductor process. In addition, all IP cores are fully parameterized, RMM compliant and validated with VSIA Quality IP metric. By selecting Noesis Technologies IP cores, you accelerate time-to-market, eliminate risk and reduce development costs.

IP Cores Portfolio

Forward Error Correction

- Reed Solomon Encoder
- Reed Solomon Decoder
- Viterbi Decoder
- Turbo Product Code Encoder
- Turbo Product Code Decoder
- Turbo Convolutional Code Encoder
- Turbo Convolutional Code Decoder
- BCH Codec
- Interleaver/Deinterleaver
- Viterbi-RS Concatenated

Encryption

- AES—FIPS PUB 197 compliant
- RC4

Networking

- E1 Framer/Deframer—ITU G.704 compliant
- T1 Framer/Deframer—ITU G.704 compliant
- HDLC controller
- I2C Master Controller
- I2C Slave Controller

Source Coding

- ADPCM Codec—ITU G.726 compliant
- A-law/ μ -law Compander—ITU G.711 compliant
- A-law/ μ -law Expander—ITU G.711 compliant

Digital Signal Processing

- Block N-Point FFT/IFFT
- Pipelined N-Point FFT/IFFT
- Soft Output Demapper
- Channel Equalizer—LMS
- Channel Interpolator—Wimax compliant

Channel Emulators

- AWGN Channel Emulator
- AWGN Channel Emulator—High Throughput

Timing Units

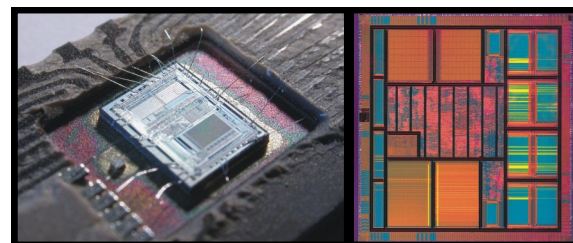
- Clock and Data Recovery

Simulators

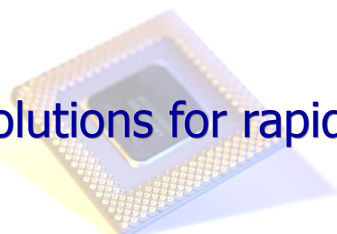
- FEC Platform

Development Systems

- ComLab



“Flexible IP Solutions for rapid SoC integration”



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