Flexible Silicon IP Core Solutions for Hardware Acceleration in SoC Era
Agenda

► Who is Noesis Technologies?
  - Company Overview

► Why choose Noesis Technologies Silicon IP Cores?
  - Competitive Advantages

► Success Stories

► Products
  - Product Highlights
  - Case Studies

► Key Markets
About Noesis

► Provider of silicon proven, process independent, fully configurable telecom IP cores for hardware acceleration.
► More than 10 years experience in IP business model.
► Based in Patras Science Park, Greece with a strong international partners network.
► IP cores that present an industry-leading combination of high performance, low power and low die-area.
► Easy customization for adaptability to a wide range of applications.
► Featuring a complete portfolio of FEC, Voice/Audio compression, Encryption, Networking and Telecom DSP IP Cores that off load demanding tasks from the CPU and drastically decrease the overall execution time.
Why Choose Noesis IP Cores?

► Minimize your Risk
  - Re-useable, fully configurable, process independent, robust IP Cores.
  - Silicon and customer proven for a variety of applications.
  - IP customization upon customer request.

► Seamless Integration
  - Supreme technical support, seamless integration.
  - Our IP developers operate as a virtual extension of customer’s engineering team.
  - 24/7 technical support via email, instant messaging or phone.

► Excellent performance
  - Various architectural characterizations optimized for high-speed, low-power and small silicon footprint.

► Facilitating Procurement Process
  - Flexible & cost-effective licensing models (RTL source or FPGA netlist).
  - IP Cores evaluation models supported by excellent pre-sales technical support.
Success Stories

ULTRA Tactical Communication Systems uses Noesis Technologies IP Cores for its family of next-generation tactical radios.

"We have purchased several IP cores under different types of licenses from Noesis Technologies. Our purchases have ranged from already developed cores to custom cores developed in conjunction with Noesis. We have been very satisfied with the functionality, delivery time, price and performance of the cores we purchased. In addition, we highly appreciated the flexibility which Noesis showed us in our interactions. This flexibility ranged from allowing us to try out cores before purchasing to excellent post-delivery support. Noesis was very accommodating to revised specs as well as various small technical demands. We feel that we are building a solid partnership with Noesis in the development of our family of next-generation tactical radios."

Phillip Sawbridge, FPGA Design Specialist, Ultra-TCS, Canada

Noesis Technologies cooperates with NASA Glenn Research Center by providing its advanced channel emulator IP Core.

"It has been great working with Noesis Technologies. The IP integration was very easy and their IP Core worked flawlessly in our system."

Monty Andro, Electronics Engineer, NASA Glenn Research Center, USA
Noesis Technologies provides its high performance Reed Solomon IP Cores to help ZyXEL Communication Corp to develop its new ECCM baseband processor for spread spectrum radio applications.

“We have worked with Noesis Technologies on several projects, and found them to consistently deliver high quality results, on or ahead of schedule.”

Kai Lee, Hardware Department Manager, Zyxel Communication Corp, Taiwan

CEM Solutions Pvt Ltd. integrates to its new line of VoIP phones Noesis Technologies advanced Audio Codec IP Cores.

“We successfully integrated Noesis Technologies Audio Codec into our VoIP product in few hours and it worked perfectly. I was also impressed by the level of their technical support. Noesis has saved us months of development time and we look forward for closer cooperation with them in our future projects.”

Rajneesh Verma, Product Line Manager, CEM Solutions Pvt Ltd., India
# IP Portfolio

<table>
<thead>
<tr>
<th>PartNumber</th>
<th>Forward Error Correction</th>
<th>PartNumber</th>
<th>Encryption</th>
</tr>
</thead>
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<td>ntRSC</td>
<td>Fully Configurable Reed Solomon Codec</td>
<td>ntAES8</td>
<td>AES Low Power Encrypt/Decrypt Engine</td>
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<tr>
<td>ntVIT</td>
<td>Fully Configurable Viterbi Decoder / Convolutional Encoder</td>
<td>ntAES32</td>
<td>AES High Speed Encrypt/Decrypt Engine</td>
</tr>
<tr>
<td>ntTPC</td>
<td>Fully Configurable Turbo Product Codec</td>
<td>ntAES128</td>
<td>AES Ultra High Speed Encrypt/Decrypt Engine</td>
</tr>
<tr>
<td>ntLDPC</td>
<td>Fully Configurable Low Density Parity Check Codec (Under Dev)</td>
<td>ntRC4</td>
<td>RC4 Encrypt/Decrypt Engine</td>
</tr>
<tr>
<td>ntBCH</td>
<td>Fully Configurable Bose Chaudhuri Hocquenghem Codec</td>
<td>ntSHA256</td>
<td>SHA 256-bit hash generator</td>
</tr>
<tr>
<td>ntINT_DEINT</td>
<td>Fully Configurable Interleaver/Deinterleaver Engine</td>
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<th>Digital Signal Processing</th>
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<tr>
<td>ntBFFT/ntPFFT</td>
<td>Block/Pipelined N-Point Fast Fourier Transform</td>
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<tr>
<td>ntCH_EST</td>
<td>Channel Equalizer</td>
</tr>
<tr>
<td>ntCH_EQ</td>
<td>Channel Estimator</td>
</tr>
<tr>
<td>ntSYNC</td>
<td>Synchronization Unit</td>
</tr>
<tr>
<td>ntSOD</td>
<td>Soft Output Demapper (Log Likelihood Ratio algorithm)</td>
</tr>
<tr>
<td>ntAWGN</td>
<td>AWGN Channel Emulator (BoX-Muller algorithm)</td>
</tr>
<tr>
<td>ntOFDM_BBP</td>
<td>OFDM Baseband Processor</td>
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<tr>
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<td>ITU-T G711 compliant 64 Kbps narrowband Voice Codec</td>
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<td>ITU-T G729A compliant 8 Kbps CS-ACELP Voice Codec</td>
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<td>ITU-T compliant E1/E2/E3 Framer/Deframer</td>
</tr>
<tr>
<td>ntT1/ntT2/ntT3</td>
<td>ITU-T compliant T1/T2/T3 Framer/Deframer</td>
</tr>
<tr>
<td>ntHDLC</td>
<td>Single Channel High Level Data Link Controller</td>
</tr>
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<td>ntl2C/AXI/SPI</td>
<td>I2C/AXI/SPI Controllers</td>
</tr>
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<th>Development Tools</th>
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<tr>
<td>ComLab</td>
<td>Integrated Development Environment for telecom systems</td>
</tr>
<tr>
<td>FecSim</td>
<td>Forward Error Correction Simulation Software</td>
</tr>
<tr>
<td>C-Cubed</td>
<td>High level synthesis tool with C and ADA frontends</td>
</tr>
</tbody>
</table>
Reed Solomon Codecs

Features
- Fully configurable, time-domain, high throughput, Reed Solomon Encoder and Decoder.
- Supports different Reed Solomon coding standards.
- Variable on the fly code rate adaptation by varying codeword length and/or number of parity symbols.
- Variable bits per symbol.
- Variable codeword length on a codeword by codeword basis.
- Variable number of errors corrected on a codeword by codeword basis.
- Supports shortened codes.
- User configured primitive polynomial.
- User configured generator polynomial.
- Supports error and erasure decoding.
- Single or multiple symbol rate clock.
- Continuous decoding with no gaps between code-words.
- Predictable decoder latency.
- Counts number of errors and flags uncorrectable codewords.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- Wireless broadband – IEEE 802.16.
- Gigabit Optical Networks (2.5, 10 & 40G) – ITU-T G.795, GPON (G.984).
- DVB (ETS 300 421 – Satellite).
- DVB (ETS 300-429 – Cable).
- ADSL (ANSI T1.413, ETS 101 388).
- DECT (ETS 300 175).
- Intelsat Earth Stations – IESS-308.
- Space Telemetry Systems.
Viterbi FEC System

Features
- Fully configurable, high throughput convolutional FEC system based on Viterbi Decoder algorithm.
- Supports different convolutional coding standards.
- Parameterizable constraint length, code rate, generator coefficients and soft bits.
- Parameterizable puncturing for full code rate control.
- Programmable traceback depth.
- Supports zero terminating and tail biting Viterbi decoding algorithm.
- Soft or hard decision decoding.
- Supports both continuous and burst input data flow.
- Supports both block and continuous based decoding.
- Fixed Viterbi decoder latency.
- Single or multiple symbol rate clock.
- Continuous decoding with no gaps between codewords.
- Predictable decoder latency.
- Area efficient design.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- 3G Wireless Base Stations.
- Wireless LAN (IEEE 802.11).
- xDSL (ADSL, VDSL, HDSL, SDSL).
- Wireless PAN (IEEE 802.15.3a).
- WiMAX (IEEE 802.16e).
- Cable Modems.
Turbo Product Codec

Features
- Programmable data block size by adjusting codeword dimensions, i.e. number of rows and number of columns.
- Supports shortening by adjusting number of rows and columns to be eliminated in order to create a shortened code.
- Programmable number of soft bits in the input data.
- 2’s complement arithmetic data format.
- Supports extended Hamming or single parity constituent codes.
- Supports (64,57), (32,26), (16,11) or (8,4) extended Hamming constituent codes.
- Supports (64,63), (32,31), (16,15) or (8,7) single parity constituent codes.
- Supports user selectable synchronous reset.
- Fixed encoder and decoder latency.
- Single edge, fully synchronous design.
- Area efficient design.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- Deep space communications.
- Optical transmission systems.
- Wireless MAN (IEEE 802.16).
Low Density Parity Check Codec
(Under Dev)

Features
● Fully configurable, high throughput, LDPC Codec Decoder.
● Supports different LDPC coding standards.
● Variable on the fly input data width, code rates, decoding iterations.
● Supports variable sub-matrix sizes (Z).
● Fully synchronous design, using single clock.

Applications
● Deep-space satellite missions (CCSDS).
● WiMax (IEEE 802.16e).
● WiFi (IEEE 802.11n - IEEE 802.11ac).
● WiGig (IEEE 802.11ad).
● WPAN (IEEE 802.15.3c).
● Hard disks.
● 10 Gigabit Ethernet - 10GBASE-T (IEEE 802.3an).
ITU-T G.975.1 I4 Super FEC Codec

Features
- 8.6 db net coding gain at 10-15 output BER.
- 10 Gbps throughput rate.
- Rich statistics including corrected bits, corrected ones, corrected zeros, corrected codewords, corrected blocks, uncorrected codewords.
- Area efficient design.
- Silicon proven in Xilinx devices.

Applications
- High bit-rate DWDM submarine systems.
- Optical transmission systems (OTU2).
(De)Interleaving Engine

Features
- Fully configurable, convolutional and rectangular interleaver / deinterleaver.
- Compliant to a variety of industry standards.
- Rectangular Block (de) interleaver function fully parameterized:
  - Block size
  - Number of rows
  - Number of columns
  - Rows and/or columns permutations
- Convolutional (de) interleaver function fully parameterized:
  - Number of branches
  - Configurable branch length
- Variable block length on a block by block basis.
- Configurable number of bits per symbol.
- Handshaking logic for I/O data flow control.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- Wireless broadband – IEEE 802.16.
- DVB (ETS 300 421 – Satellite).
- DVB (ETS 300-429 – Cable).
- ATSC.
ITU-T G711 Voice Codec

Features
- Expander expands 8 bit a-law or μ-law logarithmic PCM to 13/14 bit linear PCM.
- Compressor compresses 16 bit linear PCM to 8 bit α-law or μ-law logarithmic PCM.
- Compliant to the ITU-T G.711 standard.
- Purely combinational logic RTL implementation.
- Silicon proven in ASIC and Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- PCM codecs.
- Voice companding / expanding.
- Front-end for any DSP processing of 64 kbps voice.

The ntG711_CMP PCM to A-law transformation and PCM to μ-law transformation.

The ntG711_EXP A-law to PCM transformation and μ-law to PCM transformation.

High Performance Silicon IP Solutions
ITU-T G726 ADPCM Voice Codec

Features

- Supports 16, 24, 32 and 40 Kbps compression rates.
- ‘On-the-fly’ configuration for variable compression rate, PCM law.
- Process capability of up to 64 full duplex or up to 128 half duplex voice channels.
- Burst and continuous mode support.
- No register based configuration is required.
- A-law, μ-law linear code format selection.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications

- Cordless handsets and base stations (DECT, CT2, Cellular).
- Integrated Access Devices.
- PBX’s (Private Branch Exchange).
- Voice storage, voice mail, WAN voice processing.
- DCME (ITU G.763).
- Variable bandwidth channel.
- DSL modem, Cable modem, DSLAM.
ITU-T G729A CS-ACELP Voice Codec

Features
- Voice codec capable of multi-channel 8kbps voice compression based on ITU-T G729A standard.
- Best performance/silicon area ratio available in the industry.
- Selective Channel initialization.
- AMBA bus support for easy SoC integration.
- Fully synchronous design, using single clock.
- Portable to any FPGA/ASIC technology.

Applications
- Audio Conferencing Systems.
- Access Network Devices.
- IP Phones.
- Tele-presence Systems.
- VoIP Gateways.
- IP/PBXs.
- Voice Processors

“ntG729 provides near toll speech quality at 8 Kbps!”

High Performance Silicon IP Solutions

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CVSD Codec(1)

Applications
- 16-bit PCM Speech / Audio data Encoding / Decoding for transmission in Telecom Networks

Features
- All digital IP core design, compatible with Legacy Continuously Variable Slope Delta modulation implementations and the Bluetooth CVSD Specification.
- Programmable as either an Encoder or a Decoder.
- Programmable for 8KHz / 16KHz input data sampling frequency.
- 3,4 and 5 bits slope decision window.
- Integrated Interpolation / Decimation filters to 64KHz in order to further improve quality.
- Minimal resource utilization.
- Competitive Mean Opinion Score (MoS) when tested with ITU-T P.862 (PESQ).

Deliverables
- System netlist.
- nt_CVSD core evaluation simulation model.
- Configurable VHDL test bench with integrated test scenario.

High Performance Silicon IP Solutions
CVSD Codec(2)

System Description (Encoder – 8KHz)
- 8-times up-sampling to 64Khz.
- Digital comparator produces input comparison against a reference feedback value.
- Delta Step manager monitors past encoder decisions window to detect “slope overload” and dynamically adjusts Integrator’s delta step.
- The Integrator produces the feedback value trying to approximate the previous input value.
System Description (Decoder – 8KHz)

- Encoded input at 64Khz.
- Identical functionality as nt.CVSD Encoder, except that Digital Comparator is disabled and the Integrator’s output is the decoded output signal.
- 8-times down-sampling to 8Khz.
Performance figures

- The CVSD core has been synthesized using Xilinx ISE Design Suite. The core has been targeted to a Xilinx Virtex6 SX315t Device (package FF1156, Speed Grade -2) and the following area and performance metrics have been produced.

<table>
<thead>
<tr>
<th>CLB Slices</th>
<th>Slice LUTs</th>
<th>Slice Registers</th>
<th>DSP</th>
<th>Block RAMs</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>349</td>
<td>632</td>
<td>828</td>
<td>31</td>
<td>0</td>
<td>95 (clk64)</td>
</tr>
</tbody>
</table>

1. The implementation is speed optimized.

- Mean opinion score (MoS) when tested with 8KHz ITU-T P.862 Perceptual Evaluation of Speech Quality (PESQ).

<table>
<thead>
<tr>
<th>Bits Window</th>
<th>PESQ score</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3.2653</td>
</tr>
<tr>
<td>4</td>
<td>3.6427</td>
</tr>
<tr>
<td>5</td>
<td>3.8069</td>
</tr>
</tbody>
</table>
AES Encryption/Decryption Engines

Features
● Compliant to Advanced Encryption Standard (AES) (FIPS PUB 197).
● Supports both encryption and decryption functions.
● Supports 128/192/256-bit Cipher keys.
● Various architectures supporting throughput rates from 50 Mbps up to 12 Gbps.
● Supports ECB, CBC, CFB, OFB and CTR modes.
● Optional Key Expansion module.
● Supports I/O data flow control capability.
● Exhibits highly optimized performance-silicon area ratio.
● Fully synchronous design.
● Silicon proven in ASIC and FPGA technologies.

Applications
● Electronic financial transactions.
  - eCommerce, Banking, Securities exchange, Point-of-Sale
● Secure communications.
  - Storage Area Networks, Virtual Private Networks (VPN)
  - Video Conferencing, Voice services
● Secure environments.
  - Satellite communications, Surveillance systems, Network appliances
● Personal mobile communications.
  - Video phones, PDA, Point-to-Point Wireless
ITU-T G704 E1 Framer/Deframer

Features
- E1 framer/deframer compliant to G.704, G.706, G.732, G.775 and O.163 CCITT recommendations.
- Supports CAS and CCS signaling standards.
- Supports CRC4 based framing standards.
- User configurable receive and transmit control.
- Supports 8-bit parallel microprocessor interface for device configuration and control in host processor mode.
- Hardware control mode requires no host processor; ideal for stand-alone applications.
- Supports HDB3 line coding.
- Supports loop-back mode.
- Alarm generation, alarm detection and error logging.
- Compatible with Dallas Dallas DS2186 & DS2187 LIUs.
- Fully synchronous design.
- Silicon proven in ASIC and FPGA technologies.

Applications
- Primary rate digital trunk interfaces.
- Computer to PBX interfaces (CPI and DMI).
- High speed computer-to-computer data link
- Digital cross connect interfaces.
Performance figures
● The core has been targeted to various ASIC and FPGA technologies. The area and performance metrics produced are summarized in the following table:

<table>
<thead>
<tr>
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<th>Device</th>
<th>Resources ¹</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx</td>
<td>Spartan 3</td>
<td>1027 CLB Slices</td>
<td>102 (clk_tx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>107 (clk_rx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>207 (pclk)</td>
</tr>
<tr>
<td>Xilinx</td>
<td>Virtex 5</td>
<td>533 CLB Slices</td>
<td>280 (clk_tx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>296 (clk_rx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>475 (pclk)</td>
</tr>
<tr>
<td>Altera</td>
<td>Stratix-III</td>
<td>887 ALUTs</td>
<td>230 (clk_tx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>244 (clk_rx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>480 (pclk)</td>
</tr>
<tr>
<td>TSMC</td>
<td>0.18 um</td>
<td>9200 gates ²</td>
<td>400 (clk_tx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>432 (clk_rx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>770 (pclk)</td>
</tr>
</tbody>
</table>

¹ The implementation is speed optimized.
² Equivalent NAND2 gate count.
ITU-T G704 T1 Framer/Deframer

Features

- T1 framer/deframer compliant to G.704, G.706, G.732, G.775 and O.163 CCITT recommendations.
- Supports common framing standards.
  - 12 frames/superframe '193S'
  - 24 frames/superframe '193E'.
- Supports CRC6/non-CRC6 cases.
- Three zero suppression modes: B7 stuffing, B8ZS and transparent.
- User configurable receive and transmit control.
- Supports 8-bit parallel microprocessor interface for device configuration and control in host processor mode.
- Hardware control mode requires no host processor; ideal for stand-alone applications.
- Supports loop-back mode.
- Alarm generation, alarm detection and error logging.
- Compatible with Dallas DS2186 & DS2187 LIUs.
- Fully synchronous, silicon proven design.

Applications

- Primary rate digital trunk interfaces.
- Computer to PBX interfaces (CPI and DMI).
- High speed computer-to-computer data link
- Digital cross connect interfaces.
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<td>798 CLB Slices/12 Block RAMs</td>
<td>101 (clk_tx) 100 (clk_rx)</td>
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<tr>
<td>TSMC</td>
<td>0.18 um</td>
<td>7050 gates 2 / 4632 bits</td>
<td>432 (clk_tx) 350 (clk_rx)</td>
</tr>
</tbody>
</table>

1. The implementation is speed optimized.
2. Equivalent NAND2 gate count.
HDLC Controllers

Features
- Single port synchronous serial line interface.
- Flag/Abort Generation/Detection.
- Zero Insertion/Deletion.
- Non-octet alignment detection.
- CCITT CRC-16 Generation and Checking.
- NRZ/NRZI encoding/decoding.
- Transparent mode support.
- Receive FIFO overrun detection.
- Transmit FIFO underrun detection.
- Frame status and frame length indicators.
- Runt frame detection.
- Separate clocks for Tx and RX interfaces.
- Supports flag in interframe-time fill.
- 8-bit parallel back-end interface.
- Alarm generation, alarm detection and error logging.
- Compatible with Dallas DS2186 transmit line interface.
- Fully synchronous, silicon proven design.

Applications
- Embedded applications in Telecom systems.
- X.25 (LAPB), Q.921(LAPD) applications.
- Point to point communication links.
- ISDN, Q.922 Frame Relay, PBX, WAN.
I2C Bus Interface Controllers

Features
- Supports 3 transmission speeds:
  - normal: 100 kbps
  - fast: 400 kbps
  - high speed: 3.5 Mbps.
- Programmable clock frequency.
- Programmable acknowledge bit.
- RAM data packet buffer included with parameterized length.
- Interrupt driven data transfers.
- Supports clock stretching and wait state generation.
- Start-bit, Stop-bit, Repeated start-bit and acknowledge-bit generation.
- Multi-master operation.
- 8051 microprocessor I/F supported.
- Fully synchronous, silicon proven design.

Applications
- Suitable for a wide range of applications in telecom systems, industrial and consumer electronics, which require a cost effective serial communication channel.
- Suitable for peripherals with embedded microprocessors or microcontrollers.
FFT/IFFT Transform Processors

Features
- Fully configurable, FFT/IFFT core.
- Programmable transform type.
- Programmable transform size from 8 points to 8K points.
- 16-bit complex I/O in 2’s complement format.
- Internally generated twiddle factors.
- Supports radix2 and radix4 architecture.
- Output in natural order.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications
- Communication Systems.
- Spectrum Analysis.
- OFDM modems.
- Image processing.
- Defense Receivers and Signal Monitoring.
- Medical and Scientific Instruments.

High Performance Silicon IP Solutions
Soft Output Demodulators

Features
- Soft output demapper based on the LLR (Log Likelihood Ratio) algorithm.
- Parameterized number of soft bits per symbol.
- Parameterized architecture depending on supported modulation levels for optimum resources utilization.
- Programmable modulation level.
- Supports BPSK, QPSK, 16 QAM, 64 QAM constellations.
- Supports 2's complement of sign-magnitude soft output arithmetic format.
- Compact design that requires approximately 500 Virtex-2 CLB slices.
- Fully synchronous design, using single clock.
- Silicon proven in Xilinx FPGA technologies for a variety of applications.

Applications
- The ntSOD core can be used in any telecom application that requires an accurate and efficient log likelihood ratio method for calculating soft output information.
Clock & Data Recovery Circuits

Features

● Clock recovery from input serial data.
● NRZ data input.
● Jitter attenuation.
● Compliant with AT&T 62411 jitter transfer requirements.
● Frequency aided acquisition using external reference clock.
● Fast acquisition time.
● Narrow bandwidth Digital Phase Locked Loop.
● NCO used for an all-digital implementation.
● Programmable jitter attenuator depth for delay sensitive applications.
● Jitter generator behavioral model included.
● Fully synchronous design.
● Silicon proven in ASIC and FPGA technologies for a variety of applications.

Applications

● Sonet networks.
● Gigabit optical networks.
● Low cost datacom applications.
● Long haul telecom applications.
AWGN Channel Emulators

► Standard Version
- Fully configurable, AWGN channel noise generator.
- Generates randomly distributed bit errors.
- High accuracy by combining Box-Muller algorithm and central limit methods.
- Variable standard deviation.
- Programmable noise level.
- Normal distribution up to 4 times the standard deviation.
- Parameterized arithmetic precision.

► 12.8 Gbps High Throughput Version
- High periodicity of the generated noise samples. Period is ~ 2100.
- Probability density function (pdf) deviates less than 1% from the Gaussian pdf for |x| up to 4σ.
- Generics allow modification of arithmetic precision, number of accumulations, LFSRs initialization.
- Noise gain input is 8 bit wide with 2 bits of integer and 6 bits of fraction. Dynamic range is from 0.0 to 4.0. Step is 2-6.
- 16 bit wide noise sample (6 bits integer, 10 bits fractional part)
- Design optimized for Xilinx FPGA technology.
- Silicon proven in ASIC and FPGA technologies.
OFDM Baseband Processor

System Description
- Customized baseband processor, which implements the Physical Layer of a Time Division Duplexing (TDD) Wimax-based system, according to 802.16d standard.
- Includes both transmission and reception bit-level and symbol-level processing chains, as well as a synchronization core.
- System wrapper includes: SPI interface and controller / integrated register-file / RF interface module.
OFDM Baseband Processor

Performance figures (1)
- The ntOFDM_BBP has been synthesized using Altera Quartus II 13.1. The cores have been targeted to Altera Cyclone IV E Family FPGA “EP4CE55F23I8LN” device. The area and performance metrics produced are summarized in the following post-fit report.

```
<table>
<thead>
<tr>
<th>Top-level Entity Name</th>
<th>ntOFDM_BBP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Family</td>
<td>Cyclone IV E</td>
</tr>
<tr>
<td>Device</td>
<td>EP4CE55F23I8L</td>
</tr>
<tr>
<td>Total logic elements</td>
<td>50,140 / 55,856 (90 %)</td>
</tr>
<tr>
<td>Total combinational functions</td>
<td>43,895 / 55,856 (79 %)</td>
</tr>
<tr>
<td>Dedicated logic registers</td>
<td>24,918 / 55,856 (45 %)</td>
</tr>
<tr>
<td>Total registers</td>
<td>24918</td>
</tr>
<tr>
<td>Total pins</td>
<td>44 / 325 (14 %)</td>
</tr>
<tr>
<td>Total virtual pins</td>
<td>0</td>
</tr>
<tr>
<td>Total memory bits</td>
<td>1,336,303 / 2,396,160 (56 %)</td>
</tr>
<tr>
<td>Embedded Multiplier 9-bit elements</td>
<td>299 / 308 (97 %)</td>
</tr>
<tr>
<td>Total PLLs</td>
<td>2 / 4 (50 %)</td>
</tr>
</tbody>
</table>
```
OFDM Baseband Processor

Performance figures (2)

- BPSK - code rate RS(64,48)
- QPSK - code rate RS(32,24)

Graphs showing BER vs SNR for different scaling factors.
OFDM Baseband Processor

Performance figures (3)

![Graph showing BER vs. SNR for modulation QAM16 - code rate RS(64,43) with 1x, 2x, and 4x scaling]
Case Study: ntG729 Voice Codec

►Features

● Voice codec capable of multi-channel 8kbps voice compression based on ITU-T G729A standard

● AMBA bus support for easy SoC integration

● Portable to any FPGA/ASIC technology

● Best [performance]/[silicon area] ratio available in the industry
Performance Metrics

- Outperforms x2 an ARM CortexA9 high-end processor!
- Half the gate count compared to an ARM CortexA9 processor!
- Four times better [performance]/[silicon area] ratio compared to an ARM CortexA9 processor!
Case Study: ntG729 Voice Codec

Applications

- Audio Conferencing Systems
- Access Network Devices
- IP Phones
- Tele-presence Systems
- VoIP Gateways
- IP/PBXs
- Voice Processors
ComLab™

► Product Highlights

- ComLab is a cost efficient highly integrated development environment (IDE) that enables a system designer to rapidly build, configure and evaluate in real-time the performance of complex telecommunication systems.

- It is comprised of a Xilinx FPGA based board for the real-time HW emulation, a sophisticated application SW with interactive GUI capabilities for configuration, control and monitoring purposes as well as a rich portfolio of highly optimized telecom subsystem silicon IPs.

- ComLab platform is ideal for proof-of-concept rapid prototyping as well as an intuitive training tool for engineers.

“Noesis Technologies ComLab is a new paradigm towards communications systems hardware emulation!”
ComLab™

**Features**

- Rich portfolio of silicon optimized telecom subsystem libraries.
- Sophisticated application SW for efficient real-time performance evaluation and configuration.
- Supports graphical display capabilities of key characteristics such as BER vs SNR graphs, BER In vs BER Out graphs, Eye-Diagrams, Constellation Diagrams etc.
- Results are displayed in both graphical and tabular formats with print out, save and load capabilities.
- Can operate in a stand-alone mode or in an in-circuit emulation mode.

**Applications**

- Fast and efficient modeling and development of complex telecom systems.
- Proof-of-concept rapid prototyping.
- In-circuit emulation.
- R&D telecom engineers training.
- Educational tool for universities.
- Low-volume production.

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### Technical Data

<table>
<thead>
<tr>
<th>Telecom subsystem silicon IP libraries</th>
<th>Technical Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Error Correction (Reed Solomon, BCH, Viterbi, RS-Viterbi concatenated, Turbo product code)</td>
<td></td>
</tr>
<tr>
<td>Interleaving/Deinterleaving (Block, Convolutional)</td>
<td></td>
</tr>
<tr>
<td>Channel equalization (LMS based)</td>
<td></td>
</tr>
<tr>
<td>Modulation (PSK, QAM)</td>
<td></td>
</tr>
<tr>
<td>Soft output demodulation (LLR based)</td>
<td></td>
</tr>
<tr>
<td>Source coding (ITU-T G.726, G.711)</td>
<td></td>
</tr>
<tr>
<td>Encryption/Decryption (AES, RC4)</td>
<td></td>
</tr>
<tr>
<td>AWGN channel emulation</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Graphical Display</th>
<th></th>
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<tbody>
<tr>
<td>BER vs SNR graphs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BER In vs BER Out graphs</td>
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<td></td>
</tr>
<tr>
<td>Eye Diagrams</td>
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<td></td>
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<tr>
<td>Constellation Diagrams</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Configuration parameters</th>
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</thead>
<tbody>
<tr>
<td>Codeword sizes</td>
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</tr>
<tr>
<td>Error correction capability</td>
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<tr>
<td>Interleaving profile</td>
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<tr>
<td>Modulation level</td>
<td></td>
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<tr>
<td>SNR measurement range</td>
<td></td>
</tr>
<tr>
<td>SNR measurement step</td>
<td></td>
</tr>
<tr>
<td>BER threshold</td>
<td></td>
</tr>
<tr>
<td>Number of soft bits per symbol</td>
<td></td>
</tr>
<tr>
<td>PRBS generator length</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HW platform</th>
<th>Spartan3 Xilinx FPGA based</th>
</tr>
</thead>
</table>

| Operating System | Windows XP and higher, RS-232 interface |

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High Performance Silicon IP Solutions

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Key Markets

- Our IP cores have been successfully integrated in a wide spectrum of projects ranging from telecom, industrial control and automotive applications to defense and aerospace systems.
- World wide customer base (USA, Canada, Western Europe, India, China and Taiwan)
Clients
Network of Alliances

- Industry Associations
- Semiconductor providers
- IP portals partners
- Space Agencies
- Technical partners
- Sales partners
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